CS704 – Advanced Computer Architecture-II

Due Date: 18th May, 2012

Assignment 1

Instructions to Solve Assignments

The purpose of assignments is to give you hands on practice. It is expected that students will solve the assignments themselves. Following rules will apply during the evaluation of assignment.

- Cheating from any source will result in zero marks in the assignment.
- Any student found cheating in any two of the assignments submitted will be awarded "F" grade in the course.
- No assignment after due date will be accepted.

Question 1: Total Points (30)
Design a 16-bit ISA for processor containing the following components:

- 8 General Purpose Registers (GPR)
- ALU supporting ADD, SUB, INC, DEC, OR, XOR, AND, NAND, LSHFTR, LSHFTL, ASHFTR, and ASHFTL
- Assume ALU contains saturation and overflow check logic so support ADD and SUB with both options, i.e. overflow and saturate
- LOAD, STORE with two addressing modes Direct and Indirect
- Two control instructions Jump and Call
- NOP instruction

Design means a complete and detailed table containing bit information for every instruction. All 16-bit information must be provided to get full credit.

Question 2: Total Points (10)
In reg-mem architecture, clock cycle is 10 ns wide. It is proposed that reg-reg architecture be used instead, that reduces the clock cycle by 2 ns. However, it requires an additional load instruction, in some cases! Will the new processor be more efficient, if so under what circumstances? Quantify your answer.

Question 3: Total Points (10)
A computer architect is designing a hardware datapath implementation and the architect has determined following circuit element delays.

Instruction Memory	150 ps
Decode	70 ps
Register Fetch	60 ps
ALU	150 ps
Data Memory	200 ps
Register Write Back	60 ps

(a) What is the length of a clock cycle for a single cycle datapath implementation? (2)
(b) What would be the frequency of a processor, corresponding to single datapath implementation? (3)
(c) What would be the length of fastest clock cycle for a 5-stage pipeline datapath? What would be the corresponding processor frequency? (3)
(d) How much faster is the 5-stage pipelined datapath compared to the single cycle datapath implementation? (2)

Question 4: Total Points (20)
For the following mathematical expressions write an assembly language code:
(a) For Reg-Reg architecture (10)
(b) For Reg-Mem architecture (10)

U = A + B + D
V = C + D
W= B << 3
X = 7B + B + C+ D
Y = X + V

Question 5: Total Points (20)

Identify data hazards from the below code and show the execution of the code on a pipelined architecture on per cycle basics. You are required to highlight data hazard(s) and technique used to avoid it.

Opcode	Target	Source 1	Source 2
ADD	R1	R2	R3
SUB	R4	R1	R5
AND	R6	R1	R7
OR	R8	R1	R9
XOR	R10	R1	R11

Question 6: Total Points (10)

Read the paper title "Reducing Data Hazards on Multi-Pipelined DSP Architecture with Loop Scheduling", and answer the following question.

Describe the loop scheduling algorithm and explain how loop scheduling algorithm is better than other algorithms?